nag® *Background Paper*

NAG and Multi-core Architectures

Multi-core chips are now a mainstream reality. This is a major evolution for the industry. It is an evolution in the sense that existing codes should work seamlessly. However, many codes will not work faster, and some will even work slower than previously. Below we attempt to answer some key questions about the technology and how NAG plans to take advantage for the benefit of our users.

What is multi-core?

Put simply, more than one CPU on a chip. Currently dual-core is commonly available. That will advance to quad-core, eight-core and onwards over the next few years. In effect this is an SMP (shared memory parallel) system on a chip. Some vendors already have around 100 cores on a chip in their labs. At some point, heterogeneous cores will arrive; for example 8 'standard' cores, 4 FPGAs and 2 accelerators.

Sounds great, what's the drawback?

The challenge is that each of the cores is likely to run at a lower frequency than a single core (to reduce power and heat problems) and so any application not taking advantage of the multi-cores will likely run slower. In the past users and vendors have relied upon increases in clock speeds etc to make their applications run faster - those days are essentially at an end! Hence the challenge is to help users make good use of the multi-core technologies.

So, what is NAG doing to help me?

NAG has been working with this technology for some considerable time as part of its ongoing collaboration with the hardware vendors and researchers. In particular, as part of NAG's work with AMD to develop ACML (AMD Core Math Library), NAG has been testing and improving performance of key routines on AMD's multi-core chips. Intel has been doing similar work on their core library, MKL (Math Kernel Library). Other vendors either use these libraries or will be developing their own.

NAG encourages a building block approach to numerical problem solving and we practice what we preach. NAG libraries, wherever possible, link to the appropriate underlying vendor library (MKL, ACML, ...). This not only provides an excellent performance portability layer, but also helps future-proof against technology changes (such as multi-core). Hence, users of the NAG libraries should see performance improvements for many routines which use underlying vendor libraries.

In addition, the latest version of the NAG SMP Library (Mark 21) has a further range of routines tuned, using OpenMP, for use on multi-core and other SMP (shared memory parallel) systems. And the good news is that it has the same interfaces as the NAG Fortran Library, hence users can simply re-link and go.

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You mention SMP/OpenMP, but what about my MPI programs?

MPI is aimed mainly at distributed memory applications, but of course it can also work well within a shared memory environment. Initially it is likely that MPI versions will be available which work well in the multi-core environment as well as across distributed memory links. In the longer term, it is likely that some form of hybrid distributed/shared programming technique will be employed for best results (e.g. coarse grain-MPI parallelism and fine-grain OpenMP parallelism).

What are other vendors doing to help?

The hardware vendors will be putting a lot of effort into tools and training to help Independent Software Vendors make best use of the hardware. Hence, over time, better tools and general software will arrive.

Compiler vendors will be providing additional OpenMP support as well as other threading and performance enhancing techniques to take advantage of multi-core architectures.

So, what should I do with my programs?

Our advice is really the same as always: to use as many commercially strong components as possible to help future-proof your programs and to take advantage of the efforts of the tuning in the core vendor and NAG libraries. If you haven't done so already, we would recommend trying the NAG SMP library.

Contact NAG today.

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